Differential Voltage Current Conveyor based Low Power LNA Power LNA for Wireless Receiver

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Vivekananda Journal of Research
January - June 2021, Vol. 10, Issue 1, 108-124
ISSN 2319-8702(Print)
ISSN 2456-7574(Online)
Peer Reviewed Refereed Journal

http://www.vips.edu/vjr.php

Abstract

The use of a low-voltage PMOS bulk-driven cascade current mirror (P MOS BDCCM) to realize LNA using CMOS differential voltage current conveyor (DVCC) based on low power and free from trans-conductance variation is presented in this research paper. Just one current mirror is used in this circuit, which uses four DVCCs as active elements and two capacitors and five resistors as passive elements. The use of this active component simplifies and improves the deploymentprocess.The circuit is consuming Low Power of 1.24mW with the Voltage gain of 2.21 dB for the input voltage of 1V and seems to operate in 1- 10 GHz. The circuit's functionality is checked using Tanner simulator version 16 for a 35µm CMOS process model, and the transfer function is realized using MATLAB R2017a, yielding a variety of simulation results. To show the outcomes, simulation results are included.

Keywords: *Low Noise Amplifier, Transconductance, Bulk-driven cascade current mirror, Differential Voltage Current Conveyor (DVCC).*

INTRODUCTION

High-bit systems are becoming more common on laptop computers. In the range of GHz (typically 5-6) with data rates over many decade Mbps in the wireless system, frequency division multiplexing based modulation is most popular[1]. The linearity and dynamic range of WLAN modulations dependent on OFDM is very taxing on RF front-end

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circuits. Furthermore, low voltage RF circuits are expected to be run on broadband portable wireless systems [2].

There are significant problems with the design of these circuits. Each of the key portions of the receiver chain is the low-noise amplifier [3-4]. High-performance LNAs have been produced. However, because of its low power, cost and convergence capacity[5] the CMOS RF Chips are becoming more attractive.In this research paper, a new LNA interface circuit with a higher linearity, lower power consumption, large bandwidth is provided to CMCs using modern mode circuits.

The conventional LNA implementations are based on Voltage Mode Circuits (VMC) with operational amplifier [6-7]. These instruments have many inconveniences, such as less gain, short operational bandwidth and noise factor. These conventional devices are suffer from low band widths (BW's) arising due to stray and circuit capacitances [8-10]. However, with the advancement in the analog VLSI new analog devices are based on currents are developed called current mode circuits (CMC's) [12-13]. These circuits have a significant advantage of low power, low voltages and can operate over wide dynamic range. These circuits, CMC can offer to the designer large bandwidths, greater linearity, wider dynamic range, simple circuitry and low power consumption. Current feedback op-amps (CFOAs), operational floating conveyors (OFCs) and current conveyors (CCs) etc. are popular CMC configuration and most widely used structure among them is DVCC, extension of the second generation current conveyor (CCII). Hence, we decided to use the DVCC in the proposed scheme [14-15].

DVCC

Sedra and Smith proposed IInd generation current conveyor and also its extension in the form of Differential Voltage Current Conveyors (DVCC) [2]. The DVCC is a building block with five ports, The block symbol of DVCC shows that it has two high impedance voltage inputs: V_{Y1} and V_{Y2} and X is an input terminal with a low impedance current and two output Z_1 and Z_2 terminals with a high impedance current as shown in Fig.1.

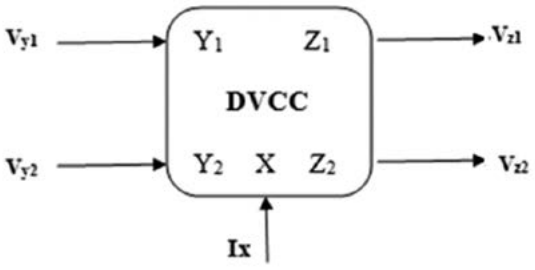

Fig. 1 DVCC Block

Matrix Representation of DVCC block is shown below

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix}$$

Input current from terminal X is followed by the output currents (I_{Z1} and I_{Z2}). The polarity of I_{Z1} is the same as that of I_X, and I_{Z2} is the opposite of I_X. Two input voltages are related to the voltage of the X terminal:

$$V_X = V_{Y1} - V_{Y2}$$

The equivalent CMOS based DVCC is shown in the Fig. 2.

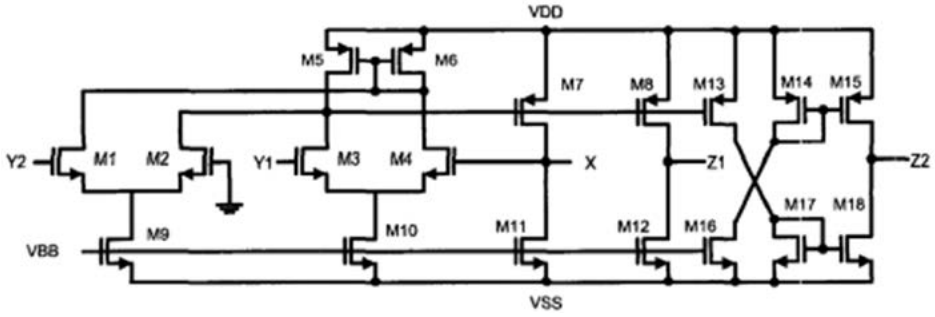

Fig2. Circuit diagram of CMOS based DVCC

The circuit realization of the proposed DVCC shown above in Fig. 2 is consisting of five terminals and the operation of the circuit is shown in the matrix formAs shown by CMOS basedDVCC configuration, all MOS transistors are operated in the saturation region with their sourceconnected with the substrate. The MOS pair M1-M2 and M3-M4 isconnected inthe differential Mode. The current through MOS Pair M1-M2 and M3-M4 formed the differential pair is mirrored with the help of M5-M6. The negative feedback operation of MOS M7 with the bias currents flowing through the transistors M9,M10 and M11 insure that the voltage at X terminal remain independent of the current withdrawn from X terminal. The current of X terminal is conveyed to Z1 terminal bymirroring action of M7 and M8. The inversion of current conveyed to terminal Z2 withthe help of mirroring action by current mirror M14-15 and M17-M18.

LNA

A cascode stage is considered one of the most common topologies for implementation of LNA circuits at multi-Gigahertz frequencies with its unprecedented advantages in terms of gains, insulation, stability and impedance matches. The typical source and common-gate transistor stacking architecture demands a comparatively high voltage in the LNA configuration and greatly deteriorates in output with the voltage of the supply declining.A folded topology was introduced for cascode LNAs for low voltage applications. Fig. 3 displays a condensed LNA folded cascode circuit schematics

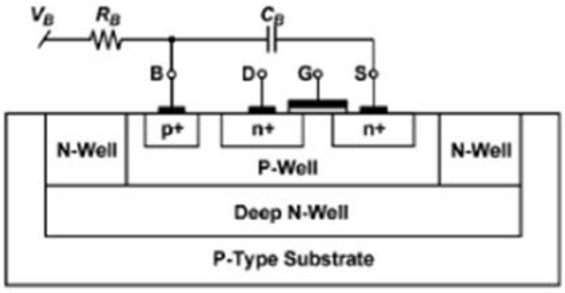

Fig.3Folded Cascode LNA schematic

The voltage of the folded cascode LNA can be decreased by one transistor overdrive because of the lack of stacking gains. The folded cascode possesses special benefits in terms of linearity of the amplifier, noise figure and reliability of bias relative to other low-voltage LNA topologies. However, one of the key issues is the inherently low gain, especially in applications that have restricted current consumption.

DEVICE DESCRIPTION

This Major Block used in the suggested scheme are

(1) DVCC-based Cascode LNA system

(2) Current follower

(3) Current Mirror for fixed bias.

The schema circuit diagram shown in Fig.4 contains 4 DVCC connected in Cascode configuration [16], 2 capacitor, 5 resistors and PMOS based bulk driven Current Mirror. Limitations of conventional system are that its transduction (gm) frequently differs with I_{bias}.

We use current mirrors along with the differential voltage current conveyors, which provide the constant I_{bias} and thus free the system from the shift of the transconducting effect, to free the device from transduction variations. There are different types of current mirrors, but the PMOS bulk-driven mirror of the cascade is used in order to make a low power version.

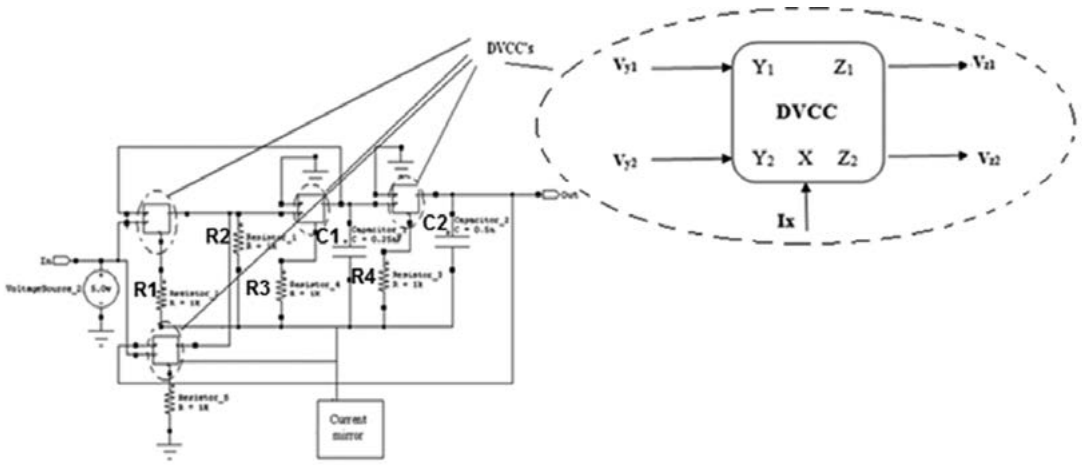

Fig.4 DVCC and passive components connections

In the Circuit shown above the DVCC are connected in such a way that Low power LNA is formed. This type of configuration is also called differential LNA and is broadly used because of its compensation of common-mode (CM) noise immunity. The selection of cascode topology within initial stage degrades the noise presentation of the amplifier yet if it improves the gain[16]. To occupied less chip area by using single ended LNAs, but if the amplifier design is single ended, it's a lot of vulnerable to noise and alternate interferences . Alternatively, by using the differential amplifier very less amount of liable to noise and intervention. Also the differential amplifier has the benefit, of getting the signal swing which will be a double that of the single-ended

GAIN/ STABILITY ANALYSIS

To perform gain analysis transfer function of the proposed scheme is calculated and shown in eq. 1

$$\frac{V_o}{V_i} = \frac{(R1(R_3+R_4)/R_1C_1R_2C_2R_3R_4)}{D(S)} \quad (1)$$

$$D(S) = S^2 + S\frac{R1}{C_1R_1R_4} + \frac{R1}{C_1C_2R_1R_2R_3} \quad `` \quad (2)$$

From (2) ω_O and Q of the proposed circuit is given as

$$\omega_O = \sqrt{\frac{R1}{R_1R_2R_3C_1C_2}}\, Q = R_4\sqrt{\frac{R_1C_1}{RR_2R_3C_2}}$$

$$\frac{V_{out}}{V_{in}} = \frac{(R1(R_3+R_4)/R_1C_1R_2C_2R_3R_4)}{S^2+S\frac{R1}{C_1R_1R_4}+\frac{R1}{C_1C_2R_1R_2R_3}} \quad (3)$$

On considering the typical value of registers and capacitors we get

$$\frac{V_{out}}{V_{in}} = \frac{12\,X10^{16}}{S^2+4\,X\,10^7S+8\,X\,10^{12}} \quad (4)$$

For stability analysis step responseanalysis, and bode plots for equation 4 is represented in Fig.5-6.

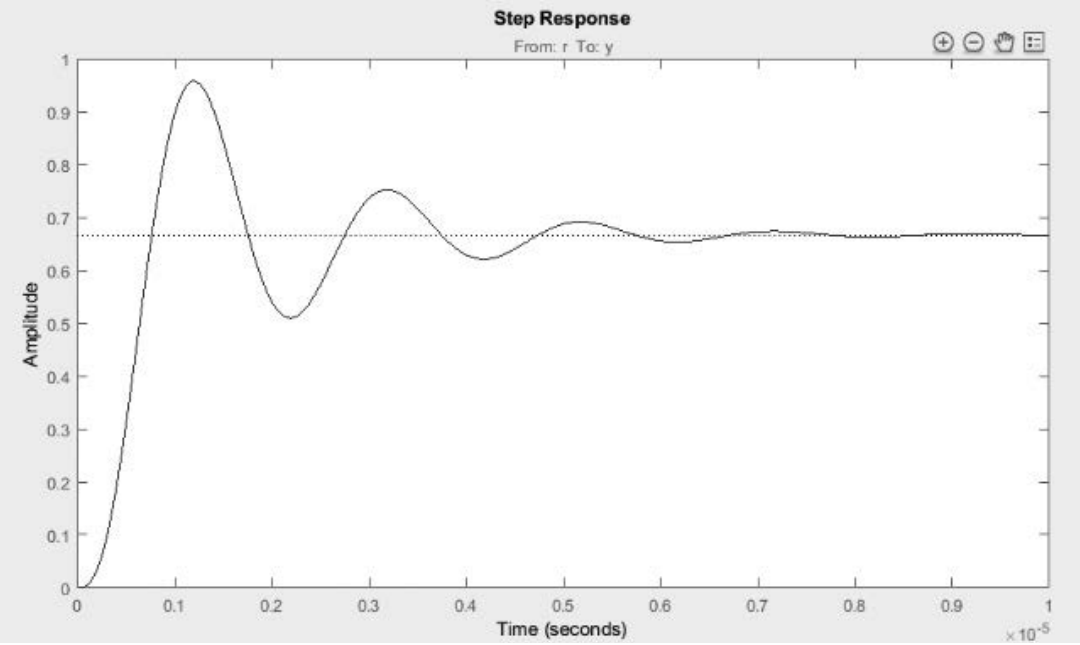

Fig.5Step response of transfer function

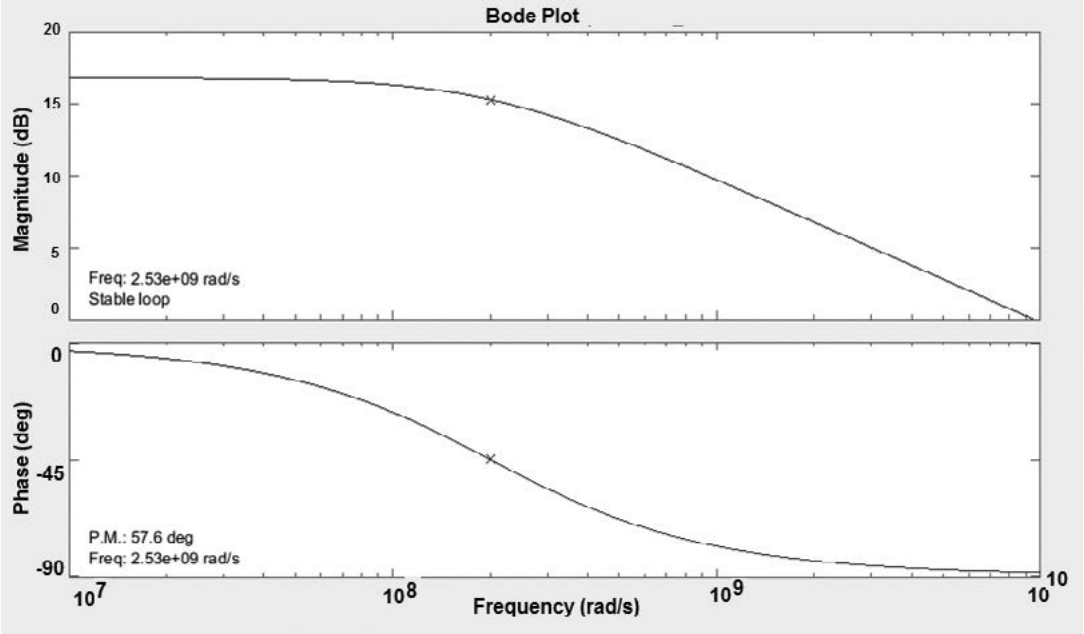

Fig.6 Bode plot of transfer function

By observing above figure it is justify that the TF shown in equation 4 of the system is stable in closed loopwith phase margin of 57.6 degree and infinite gain margin. Also it is observed that the Max Gain of 17 dB at 2.5 GHz when operating in the range of 1 to 10 GHz. This shows the Voltage gain is decreases gradually when operating in a high frequency which may be due to intervening of parasitic capacitance at high frequency.

PMOS BULK-DRIVEN CASCADE CURRENT MIRROR

For low power design and to make the system independent of trans conductance effect a PMOS based BDC current mirror is used in order to fix the bias current (I_{bias}) [17]. The structure of same is givenbelow in Fig.7

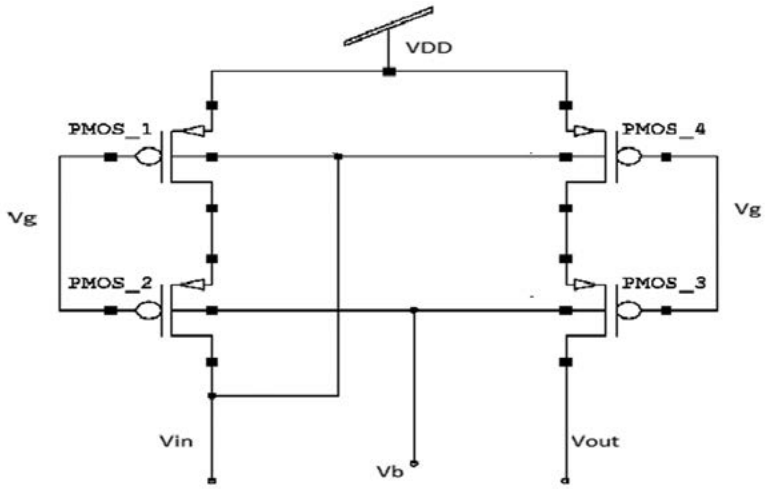

Fig.7 BDC Current Mirror

The mathematical expression for minimum and maximum output voltage drop is

$| V_{dd} - V_{in} |_{(min, BD)} = V_{SB1} = V_{SD1} + V_{SD2}$

$| V_{dd} - V_{out} |_{(min, BD)} = V_{SD3} + V_{SD4}$

$| V_{dd} - V_{in} |_{(min, GD)} = V_{SG} = V_{on} + V_T$

$| V_{dd} - V_{out} |_{(min, GD)} = 2V_{SD,sat}$

The input voltage drop of BDCCM is

$| V_{dd} - V_{in} |_{(min, GD)} = V_{SB1} \leq 0.29$

This is much lower than Gate driven current mirror.

Also for BDCCM

$V_{SG1} > V_{SG2}$ and $I_{SD1} = I_{SD2}$

Forcing >

$V_{SB} => V_{DD} - V_{SD1} - V_b \leq 0.29$

Hence $V_b \geq V_{DD} - V_{SD1} - 0.29$

for $V_{SB1} = V_{SB3}$ and $V_{SG1} = V_{SG3}$ then $I_{SD1} = I_{SD3}$

If M3 also were in linear region $V_{SD1} = V_{SD4}$

Since M4's source drain voltage is unregulated, the BDCCM minimum output voltage drop can be apparent to M4 in linear or saturation area lower than that of the GDCCM. The bulk powered technology will essentially remove the threshold voltage constraint hence minimizing the CMOS analog IC voltage requirement. The low-voltage BDCCM decreases the input/output voltage drop considerably compared to standard gate-driven CMs and has a reasonable input/output resistance function along with a better driving power for current.

COMPARISON

The comparison of proposed design is given in Table 1. It is clearly observed that the device consumes very less power in order of 1,24 mW as compared to the other conventional devices. The graphical representation of the same is shown in Figure 13

Table 1 comparison with existing Devices

[Ref]	Power (mW)	Gain (dB)	F0 (GHz)
[6]	**30**	**22**	**1.5**
[7]	**12**	**22**	**2.5**
[8]	**22.4**	**19.8**	**2.4**
Proposed design	**1.24**	**17**	**1-10**

Inference from Table 1

Proposed DVCC based LNA design simulation are carried out in Tanner Tool of Mentor Graphics using 0.35 μm CMOS process technology.

When we compare the latest design to the old design, we get the following findings.

(a) The average power consumption obtain through the simulation is 1.24mW which is 2 % when compared with the other conventional circuits mentioned in reference [6], [7], [8] and the same is included in the Appendix as a reference

(b) Also it is observed that the Max Gain of 17 dB at 2.3 GHz when operating in the range of 1 to 10 GHz. This shows the Voltage gain is decreases gradually when operating in a high frequency which may be due to intervening of parasitic capacitance at high frequency.

(c) The operating frequency range of the device is 1 to 10 GHz which makes it suitable for wide band receivers applications.

RESULT

Simulation of low power LNA for wireless receiver with DVCCand PMOS based bulk driven cascade current mirror in order to make it independent of trans conductance effect is presented in this paper. MATLAB and Tanner tool 16 are the tool used for the calculation of result. In the practical high performance LNA , together with a wanted signal, radio receiver detects also unwanted components of the spectrum, in most cases having average power much larger than that of the signal of interest. This would not represent a serious problem if the receiver was a linear system (and not limited by maximum power supply voltages and currents), having ability to process signal of any strength with constant performance. The device is highly linear as indicated in Fig. 9which indicate it is more immune to noise and signal generated by other unwanted component of spectrum. The device consumes low power in the order of 1.24mW and the results are included in the appendix at the end of the paper. Also the ac analysis shown in Fig.10 that device can be operated in the 1- 10 GHz range with a voltage gain of 17 dB as obtain from bode plot. The device is stable as indicated in gain and stability section.The VHDL file corresponding to the DVCC is exported using Tanner Tool and the RTL and technology diagram thus obtained is shown in Fig. 11 and 12. Designers use a Register-Transfer Level(RTL) description of the design to make optimizations and trade-offs very early in the design flow.The presence of functional blocks in an RTL description makes the complexity of architectural design much more manageable even for large chips because RTL has granularity sufficiently larger than gate- or circuit-level descriptions. The synthesis file is also included in the appendix

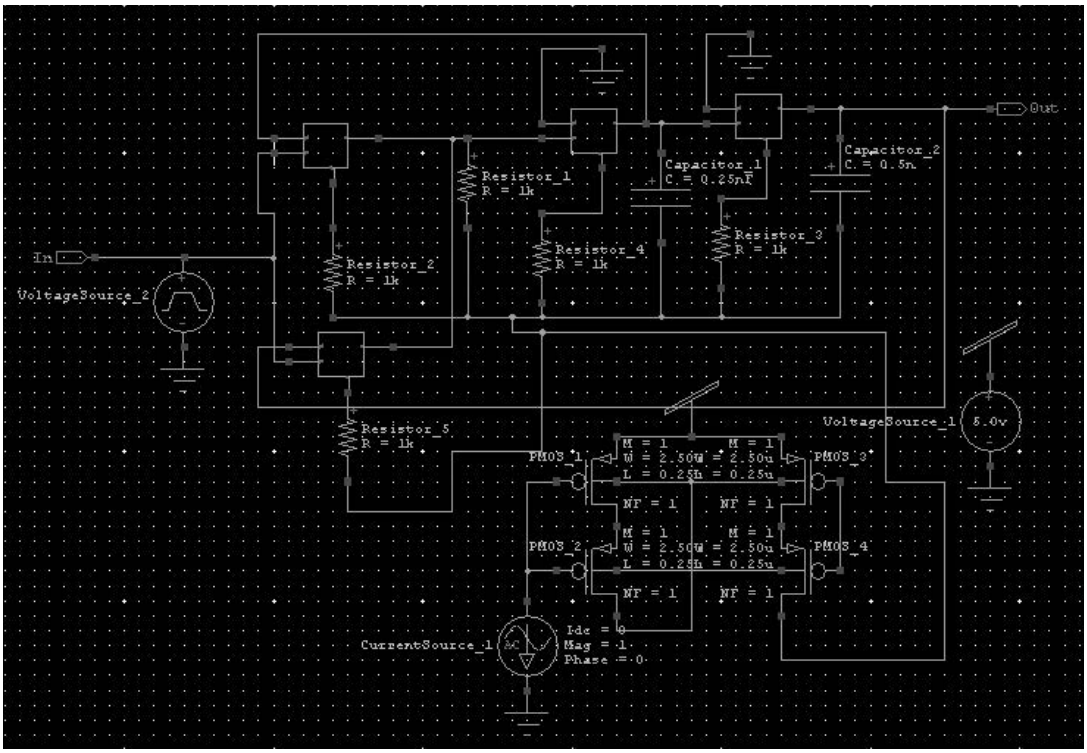

Fig.8 proposed scheme

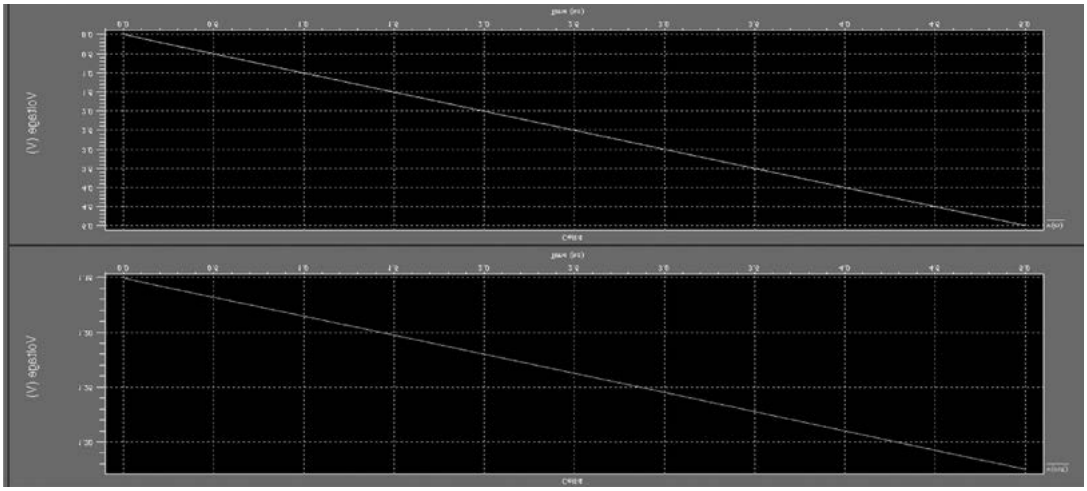

Fig.9variation of output w.r.t time.

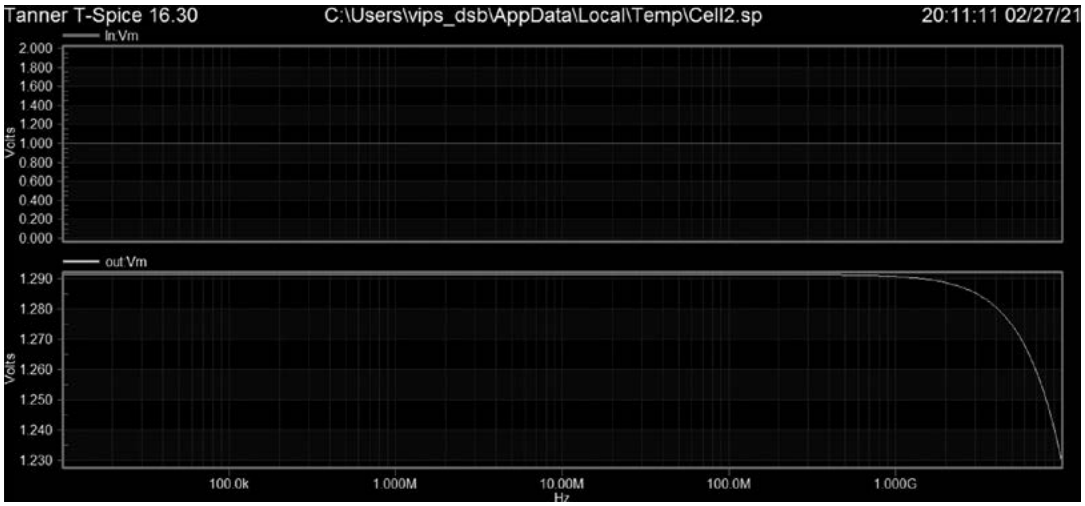

Fig 10. Frequency analysis

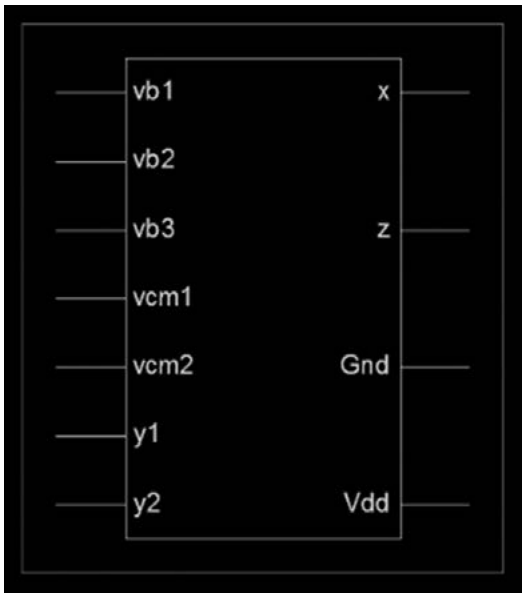

Fig. 11 RTL of DVCC

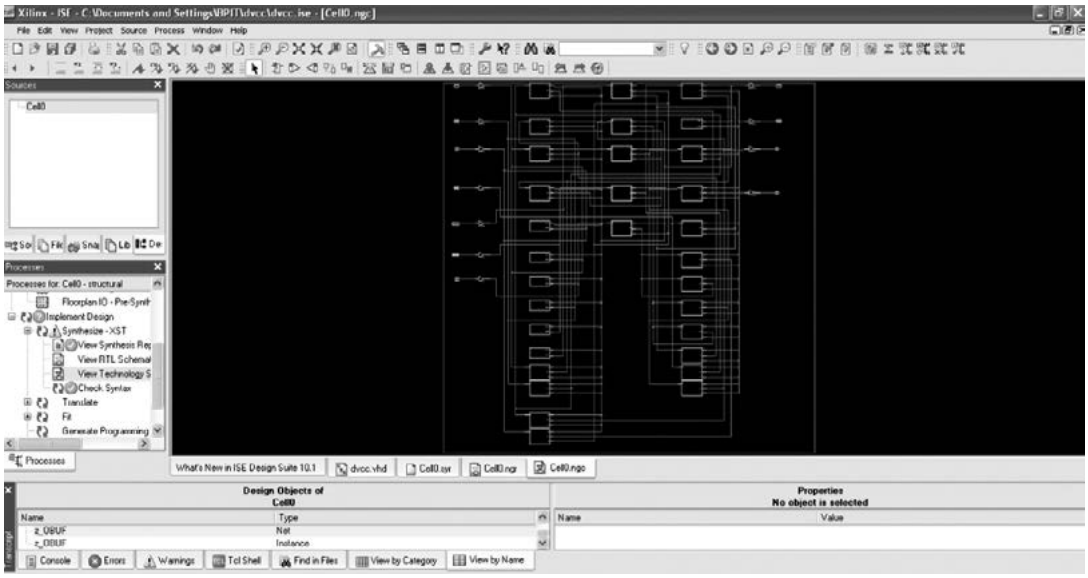

Figure 12 Technology diagram of DVCC

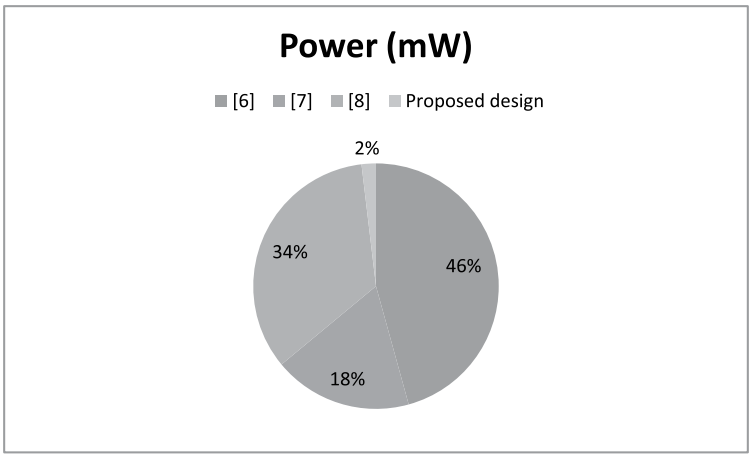

Figure 13Power consumption analysis

CONCLUSION

This paper proposes a new LNA based on CMOS differentialcurrent transmitters (DVCCs). The large-scale technology to measure the DVCC transconducting effect would lower the voltage threshold and lower the supply voltage used by CMOS analogue IC. Software simulation results and research data comparisons and transistor-level simulations

have shown the excellence of this process. The simulation and interpretation is consistent with all the results.

FUTURE SCOPE

One significant advantage of the proposed strategy is that this method is insensitive and highly adaptive to the transconductance impact. It is possible to generalize this analysis, and to make more power and size improvements at the layout level, providing better results.

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APPENDIX

T-Spice - Tanner SPICE

Version 16.30

Power Results
Average power consumed -> 1.245160 e-003 watts
Max power 1.245160e-003 at time 3.93375 e-007
Min power 1.245160e-003 at time 5e-007

Parsing 0.03 seconds

Setup	0.01 seconds
Transient Analysis	0.36 seconds
Overhead	0.72 seconds
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Total	1.13 seconds

Simulation completed

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* Synthesis Options Summary *

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---- Source Parameters

Input File Name	: “Cell0.prj”
Input Format	: mixed
Ignore Synthesis Constraint File	: NO

---- Target Parameters

Output File Name	: “Cell0”
Output Format	: NGC
Target Device	: Automotive 9500XL

---- Source Options

Top Module Name	: Cell0
Automatic FSM Extraction	: YES
FSM Encoding Algorithm	: Auto
Safe Implementation	: No
Mux Extraction	: YES
Resource Sharing	: YES

---- Target Options

Add IO Buffers	: YES
MACRO Preserve	: YES
XOR Preserve	: YES
Equivalent register Removal	: YES

---- General Options

Optimization Goal	: Speed
Optimization Effort	: 1

Library Search Order	: Cell0.lso
Keep Hierarchy	: YES
Netlist Hierarchy	: as_optimized
RTL Output	: Yes
Hierarchy Separator	: /
Bus Delimiter	: <>
Case Specifier	: maintain
Verilog	: YES
---- Other Options	
Clock Enable	: YES
wysiwyg	: NO

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